

III. REMARKS

Claims 1-20 are pending in this application. By this Amendment, claims 1 and 8 have been amended. Applicant does not acquiesce in the correctness of the rejections and reserves the right to present specific arguments regarding any rejected claims not specifically addressed. Further, Applicant reserves the right to pursue the full scope of the subject matter of the original claims in a subsequent patent application that claims priority to the instant application. Reconsideration in view of the following remarks is respectfully requested.

In the Office Action, claims 5-7, 13-14, 16-17 and 19-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant gratefully appreciates this indication.

In the Office Action, claims 1-4 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Schneider (U.S. 6,201,829), in view of Drost et al. (U.S. 6,076,175), hereafter “Drost,” and Variyam et al. (U.S. 6,661,266), hereafter “Variyam”; claims 8-11, 15 and 18 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Ramamurthy et al. (U.S. 5,787,114), hereinafter “Ramamurthy,” in view of Drost; and claims 12-13 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Ramamurthy and Drost, and in view of Variyam. Applicant respectfully submits that the claimed subject matter is allowable for the reasons stated below.

Applicant submits that the suggested combinations of the cited prior references do not teach or suggest each and every feature of the claimed invention. For example, with regard to independent claim 1, the suggested combination of Schneider, Drost and Variyam does not

disclose or suggest, *inter alia*, “a built-in-self-test (BIST) device ... for providing a clock signal with varied offset for jitter testing the transceiver[.]” (Claim 1). As the Office directly and indirectly admits, Schneider and Drost do not include “providing a clock signal with varied offset[.]” (*See* Office Action at page 3.) Contrary to the assertion of the Office, Applicant submits that Variyam also does not disclose or suggest this feature. Rather, Variyam discloses a BIST circuit “for measuring error of a phase lock loop output clock signal.” (Col. 3, lines 18-19). In Variyam, “a short pulse is generated from the PLI output” (col. 6, lines 43-44, *emphasis added*), “delayed by passing them through the delay chain 210” (col. 7, lines 1-2), and compared against the PLI clock output” (col. 7, line 11, *emphasis added*) to measure errors of the PLI clock output. As such, Variyam does not provide the delayed short pulses for jitter testing the PLL. Instead, Variyam attempts to measure the jitters that already exist in the PLI output. Variyam does not generate an output signal corresponding to the PLI output and the delayed short pulses. In view of the foregoing, the combination of Schneider, Drost and Variyam does not disclose or suggest “a built-in-self-test (BIST) device ... for providing a clock signal with varied offset for jitter testing the transceiver[.]” Accordingly, Applicant respectfully requests withdrawal of the rejection.

The above arguments also apply to claims 8, 15 and 18, as claims 8, 15 and 18 include “varying an offset of a clock signal embedded within the network data signal[.]” Applicant submits that Ramamurthy does not overcome this deficiency of Drost.

The dependent claims are believed allowable for the same reasons stated above, as well as for their own additional features

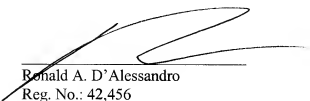
IV. CONCLUSION

In light of the above, Applicant respectfully submits that all claims are in condition for allowance. Should the Examiner require anything further to place the application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the number listed below.

Respectfully submitted,

Date:

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